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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,378	11/14/2006	Toshiyuki Asahi	2006_0040A	6101
52349	7590	05/15/2007	EXAMINER	
WENDEROTH, LIND & PONACK L.L.P.			RAO, SHRINIVAS H	
2033 K. STREET, NW			ART UNIT	PAPER NUMBER
SUITE 800			2814	
WASHINGTON, DC 20006			MAIL DATE	DELIVERY MODE
			05/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/565,378	ASAHI ET AL.
	Examiner	Art Unit
	Steven H. Rao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 06 April 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-25 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 01/05/2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 01/21/2006
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application
 6) Other: _____.

DETAILED ACTION

Priority

Acknowledgement is made of papers filed claiming priority from PCT/NL2004-000507 filed on July 13, 2004 which itself claims priority from Japanese Patent Application Nos. 2003-279110 filed July 24, 2003 and 2003-321325 filed on November 12, 2003.

Information Disclosure Statement

The Ids filed on 01/13/2006 has been considered and the initialed copy of the PTO-1449 made of record.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rathburn (U.S. Patent Application Publication No. 2003/0003779 (now US Patent No. 6,939, 143) in view of Takaishi (U.S. Patent Publication No. 2003/0209792 now U.S. Patent No. 7,002,237, herein after Takaishi, in the rejection below references are to portions of the issued patent only).

With respect to claim 1 Rathburn describes a wiring board (figs.13, etc. 206) which comprises at least one spherical semiconductor element (214), an electrically insulating substrate (figs. 20) and a predetermined

wiring pattern which is located on each main surface of the electrically insulating substrate (210,212).

Rathburn describes a plastic/organic substrate , but does not specifically mention its plastic/organic material to be a resin.

However , Takaishi a patent from the same field of endeavor describes in figures and col. 3 lines 27-28, etc. the substrate of resin to provide a spherical semiconductor device and a mounting method with efficient connection openings for mounting and provides highly reliable connection with a printed circuit substrate.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include resin substrate in place of Rathburn's plastic/organic material substrate.

The motivation for the above combination is to provide a spherical semiconductor device and a mounting method with efficient connection openings for mounting and provides highly reliable connection with a printed circuit substrate. (Takaishi col.2 lines 49-55).

The remaining limitations of claim 1 are :

and the wiring pattern formed on one main surface of the electrically insulating substrate and the wiring pattern formed on an opposite main surface are electrically connected through a wiring formed on a surface

of the spherical semiconductor element (fig. 13 , 210,212 connected thru'214), and the spherical semiconductor element is embedded at least partially in the electrically insulating substrate. (figs.12c, 19, 20, etc.).

With respect to claim 2 Rathburn describes the wiring board according to claim 1 wherein the wiring patterns on the both main surfaces of the electrically insulating substrate are also connected by means of a via hole conductor which is provided in the electrically insulating substrate. (fig. 12c, para 0076).

With respect to claim 3 Rathburn describes the wiring board according to claim 1 wherein a passive element and/or an electronic part is further embedded in the electrically insulating substrate.(fig. 17).

With respect to claim 4 Rathburn describes the wiring board according to claim 3 wherein at least one of the wiring pattern formed on one main surface of the electrically insulating substrate and the wiring pattern formed on an opposite main surface is connected to the passive element and/or the electronic part through the via hole conductor. (fig. 17)

With respect to claim 5 Rathburn describes the wiring board according to claim 1 wherein a portion of the spherical semiconductor element is

exposed from the electrically insulating substrate and a bump is formed on a periphery of the exposed spherical semiconductor element above the electrically insulating substrate, the wiring patterns formed on the main surfaces of the electrically insulating substrate and the wiring of the spherical semiconductor element are connected through the bump.

With respect to claim 6 Rathburn describes the wiring board according to claim 1 wherein the electrically insulating substrate is a transparent substrate. (Takaishi col. 3 line 41-2-polyimide –the same transparent material also used by applicants' see claim 15 herein below , etc.) .

With respect to claim 7 Rathburn describes the wiring board according to claim 1 wherein the electrically insulating substrate is made of a mixture which contains an inorganic filler and a thermoset resin. (Rathburn col. 2, Takaishi col.6 lines 51 to 64)

With respect to claim 8 Rathburn describes the wiring board according to claim 1 wherein it comprises other spherical element which is made of an electrically insulating material in addition to the spherical semiconductor element.(takaishi figs. #14, col. 10 line 66-protective insulating film) .

With respect to claim 9 Rathburn describes the wiring board according to claim 1 wherein a plurality of the spherical semiconductor elements

are embedded such that they are arranged along a thickness direction of the wiring board. (figs. 13,19 20 etc.).

With respect to claim 10 Rathburn describes the wiring board according to claim 1 wherein the electrically insulating substrate further comprises at least one layer of a wiring pattern in its inside, whereby the wiring board is a multilayer wiring board. (Fig. 13, #026-multilayer-para 077).

With respect to claim 11 Rathburn describes the wiring board according to claim 1 wherein at least a portion of the wiring board is flexible.(Rathburn-title, abstract line 1, etc.).

With respect to claim 12 Rathburn describes the wiring board according to claim 1 wherein the wiring board is composed of a plurality of wiring board parts which have different flexibilities respectively. (para 0074)

With respect to claim 13 Rathburn describes the wiring board according to claim 12 wherein the different flexibilities are provided by a rigidizing element(s) which is present in the electrically insulating substrate. (para 0074).

With respect to claim 14 Rathburn describes the wiring board according to claim 1 wherein at least one of the wiring patterns on the main surfaces of the electrically insulating substrate comprises a terminal of

an electronic part which is located on the main surface of the electrically insulating substrate. (fig.10 A, para 0064).

With respect to claim 15 Rathburn describes the wiring board according claim

1 wherein the electrically insulating substrate of the wiring board is made of a resin composition which contains as its main component at least one elected from the group consisting of a polyimide resin, (Takaishi 3 lines 27-28) a wholly aromatic polyamide resin, an epoxy resin, a phenol resin, a wholly aromatic polyester resin, an aniline resin, a polydiphenyl ether resin, a polyurethane resin, a urea resin, a melamine resin, a xylene resin, a diallyl phthalate resin, a phthalic resin, a fluororesin, and a liquid crystal polymer. (Takaishi col. 6 lines 5-60).

With respect to claim 16 Rathburn describes the wiring board according to claim 15 wherein the resin composition contains at least one inorganic filler selected from the group consisting of alumina, silica, aluminum nitride, boron nitride, and magnesium oxide. (Takaishi col. 6 line 53).

With respect to claim 17 Rathburn describes the wiring board according to claim 16 wherein the inorganic filler has coatings on its particle surfaces which coatings made of a saturated or unsaturated fatty acid.

With respect to claim 18 Rathburn describes the wiring board according

to claim 1 wherein it has a notch in its periphery. (Rathburn figure 16).

With respect to claim 19 Rathburn escribes an electronic device which comprises the wiring board according to claim 1. (Rathburn para 0002).

With respect to claim 20 Rathburn describes a process of producing a wiring board which contains a spherical semiconductor element, comprising at least the steps of:

(I-a) embedding the spherical semiconductor element totally in a prepreg substrate which is made of a curable resin composition in its uncured condition; (Takaishi col. 6 lines 60-65)

(I-b) forming respectively, on carrier sheets, bumps and wiring patterns which are to be connected through a wiring of the spherical semiconductor element so as to obtain an upper wiring pattern transfer material and a lower wiring pattern transfer material; (Rathburn fig. 17, Takaishi fig.1 etc.).

(1-c) locating and aligning each of the above mentioned wiring pattern transfer material, through a resin sheet in its uncured condition, on each side of the prepreg substrate in which the spherical semiconductor element is embedded, followed by heating with pressing so as to integrally bond them, whereby the prepreg substrate and the uncured resin sheets are made into an electrically insulating substrate while the wiring patterns are connected with the wiring of the spherical semiconductor element; (Rathburn paras 0049 to 58, Takashi

col. 7 lines 7 to 15) and (l-d) removing the carrier sheets and leaving the wiring patterns and the bumps on the electrically insulating substrate so as to transfer them. (Rathburn paras 0064 to 0068, Takaishi col. 7 lines 60 to col. 8 lines 9).

With respect to claim 21 Rathburn describes a process of producing a wiring board which contains a spherical semiconductor element, comprising at least the steps of : (2-a) embedding a portion of the spherical semiconductor element in a prepreg substrate which is made of a curable resin composition in its uncured condition, so that a portion of the spherical semiconductor element is exposed above at least one main surface of the prepreg substrate ; (Takaishi col. 6 lines 60-65) (2-b) forming respectively, on carrier sheets, bumps and wiring patterns which are to be connected through a wiring of the spherical semiconductor element so as to obtain an upper wiring pattern transfer material and a lower wiring pattern transfer material, provided that as to the transfer material which is, in the following step (Rathburn paras 0064 to 0068, Takaishi col. 7 lines 60 to col. 8 lines 9). (2-c), placed on a side of the prepreg substrate on which side the portion of the spherical semiconductor element is exposed, a hole is also formed through the carrier sheet which hole such portion is able to pass through; (Rathburn paras 0064 to 0068, Takaishi col. 7 lines 60 to col. 8 lines 9) (2-c) locating and aligning

each of the above mentioned wiring pattern transfer sheets, through a resin sheet in its uncured condition provided that a hole is formed through the resin sheet which is to be placed on the side of the prepreg substrate on which side the portion of the spherical semiconductor element is exposed), on each side of the prepreg substrate in which the spherical semiconductor element is embedded while the exposed portion of the spherical semiconductor element is located through the holes of the carrier sheet and the resin sheet, followed by heating with pressing them so as to integrally bond them, whereby the prepreg substrate and the uncured resin sheets are made into an electrically insulating substrate while the wiring patterns are connected to each other with the wiring of the spherical semiconductor element; and(Rathburn figure 10 etc. , Takashi (Rathburn paras 0064 to 0068, Takaishi figures , col. 7 lines 60 to col. 8 lines 9). (2-d) removing the carrier sheets and leaving the wiring patterns and the bumps on the electrically insulating substrate so as to transfer them. (Rathburn figures 10, Takaishi figures, e.g 10)

With respect to claim 22 Rathburn describes a process of producing a wiring board comprising at least the steps of:

(3-a) embedding at least a portion of a spherical semiconductor element in a prepreg substrate which is made of a curable resin composition in its uncured condition, and also embedding a passive element having terminal electrodes

at its both ends respectively; (Ratnburn figure 10, Takaishi figure figures including 5)(3-b) forming respectively, on carrier sheets, bumps and conductive thin layers as well as wiring patterns which are to be connected to each other through a portion of the wiring of the spherical semiconductor element which portion is exposed so as to obtain an upper wiring pattern transfer material and a lower wiring pattern transfer material; (Rathburn figs. Including 17, Takaishi figures including 4a, etc.) (3-c) locating and aligning each of the above mentioned wiring pattern transfer materials, through a resin sheet in its uncured condition provided that a hole is formed through a region of the resin sheet which region is to face the conductive thin layer when the transfer material is so located and aligned, on each side of the prepreg substrate in which the spherical semiconductor element is embedded while the conductive thin layers are located on the terminal electrodes of the passive element, followed by heating with pressing them so as to integrally bond them, whereby the prepreg substrate and the uncured resin sheets are made into an electrically insulating substrate while the wiring patterns are connected to each other with the wiring of the spherical semiconductor element; (Rathburn paras 0064 to 0068, Takaishi figures , col. 7 lines 60 to col. 8 lines 9 and (3-d) removing the carrier sheets and leaving the wiring patterns and the bumps on the electrically insulating substrate so as to

transfer them. (Ratnburn fig. 10 , etc.).

With respect to claim 23 Rathburn describes a process of producing a wiring board in which a spherical semiconductor element is used, comprising at least the steps of: (4-A) providing the spherical semiconductor element having a wiring on its surface (Rathburn fig. 10, Taikaishi fig. 1, etc.) ; (4-B) embedding a passive element in the form of a chip having a terminal electrode at its each end in each prepreg substrate which is made of a curable resin composition in its uncured condition, so that a part embedded upper prepreg substrate and a part embedded lower prepreg substrate are obtained ; (Takashi fig. 4A , etc.) (4-C) forming a space in a predetermined position in each of the part embedded upper prepreg substrate and the part embedded lower prepreg substrate; (Rathburn fig. 16) (4-D) forming respectively, on carrier sheets, conductive thin layers and wiring patterns which are to be connected to each other by the wiring of the spherical semiconductor element, so that an upper transfer material and a lower transfer material are obtained; (rathburn figures, Takaishi fig. 4A) (4-E) locating a resin sheet in its uncured condition in at least one of a space between the part embedded upper prepreg substrate and the part embedded lower prepreg substrate, a space between the part embedded upper prepreg substrate and the upper transfer material and a space between the part embedded lower prepreg substrate and the

lower transfer sheet, and also locating the spherical semiconductor element between the part embedded upper prepreg substrate and the part embedded lower prepreg substrate, followed by aligning all of them; (Rathburn figs. , Takashi fig.1,4a,5 ,etc.) (4-F) heating so as to bond the transfer sheets, the prepreg substrate, and the resin sheets while pressing them together so as to make the prepreg substrate and the resin sheets into an electrically insulating substrate while connecting the passive element to the wiring of the spherical semiconductor element; (see rejection above e.g 3c) and (4-G) removing the carrier sheets and leaving the wiring patterns and the bumps on the electrically insulating substrate so as to transfer them. (see rejection above e.g 3d).

With respect to claim 24 Rathburn describes a process of producing a wiring board which contains a spherical semiconductor element, comprising at least the steps of: (5-1) providing a transfer material by forming a predetermined first wiring pattern on a carrier sheet; (5-2) mounting, on a predetermined position of the first wiring pattern of the transfer material, at least one spherical semiconductor element having a wiring on its surface so as to provide a first transfer material; (5-3) providing a second transfer material by forming a predetermined second wiring pattern on a carrier sheet; (5-4) superimposing a prepreg substrate made of a uncured resin composition and

the two transfer materials such that the first wiring pattern and the second wiring pattern are opposed through the prepreg substrate, followed by pressure bonding them at a heated temperature under an elevated pressure, so that the spherical semiconductor element is embedded into an electrically insulating substrate while the first wiring pattern and the second wiring pattern are connected by the wiring of the spherical semiconductor element; and (5-5) removing the carrier sheets so as to transfer the first wiring pattern and the second wiring pattern. (rejected for reasons set out under claims 20-23 above).

With respect to claim 25 Rathburn describes a process of producing a wiring board which contains a spherical semiconductor element, comprising at least the steps of: (6-1) providing a first carrier sheet comprising a first metal layer on its surface; (6-2) mounting, on a second metal layer placed on a surface of a second carrier sheet, at least one spherical semiconductor element having a wiring on its surface; (6-3) superimposing while aligning the first carrier sheet and the second carrier sheet such that their metal layers are opposed to each other through a prepreg substrate made of an uncured resin composition, followed by pressure bonding them at a heated temperature under an elevated pressure, so that a laminate is obtained in which the spherical semiconductor element is embedded into an electrically insulating substrate while the first metal layer and the second metal layer are connected to the

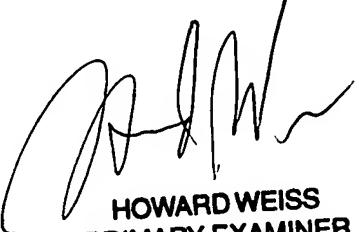
spherical semiconductor element; and (6-4) removing the first carrier sheet and the second carrier sheet from the laminate, followed by processing as predetermined to obtain a first wiring pattern a the second wiring pattern. (rejected for reasons setout under 20-24 above).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Steven H. Rao
Patent Examiner
May 6 2007


HOWARD WEISS
PRIMARY EXAMINER